

## Introduction

The Stratix® III family of devices from Altera® is based on 65-nm technology and uses the most advanced architecture and power saving techniques. These power saving techniques cover a variety of process, circuit, and architecture optimizations and innovations. Stratix III devices are based on a 1.1 V core voltage, triple-gate oxide, all-copper routing 65-nm process technology with low-k dielectric material that dramatically reduces power and improves performance. Stratix III devices include advanced, efficient logic structures called adaptive logic modules (ALMs) that obtain maximum performance while minimizing power consumption.

Altera provides the Quartus® II PowerPlay Power Analyzer tool to aid you during the design process by delivering fast and accurate estimations of power consumption. You can use this information to locate the blocks in your design that are consuming the most power and target those blocks to minimize the power consumption of your design.



For more information about the PowerPlay Power Analyzer, refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

## Designing for Low Power

Total FPGA power consumption consists of I/O power, core static power, and core dynamic power. This application note focuses on design optimization options and techniques that help reduce core dynamic and core static power in Stratix III devices. These techniques include:

- [Selectable Core Voltage](#)
- [Programmable Power Technology](#)
- [Device Selection Considerations](#)

This application note describes these power optimization techniques in detail and provides information about how to use them effectively.

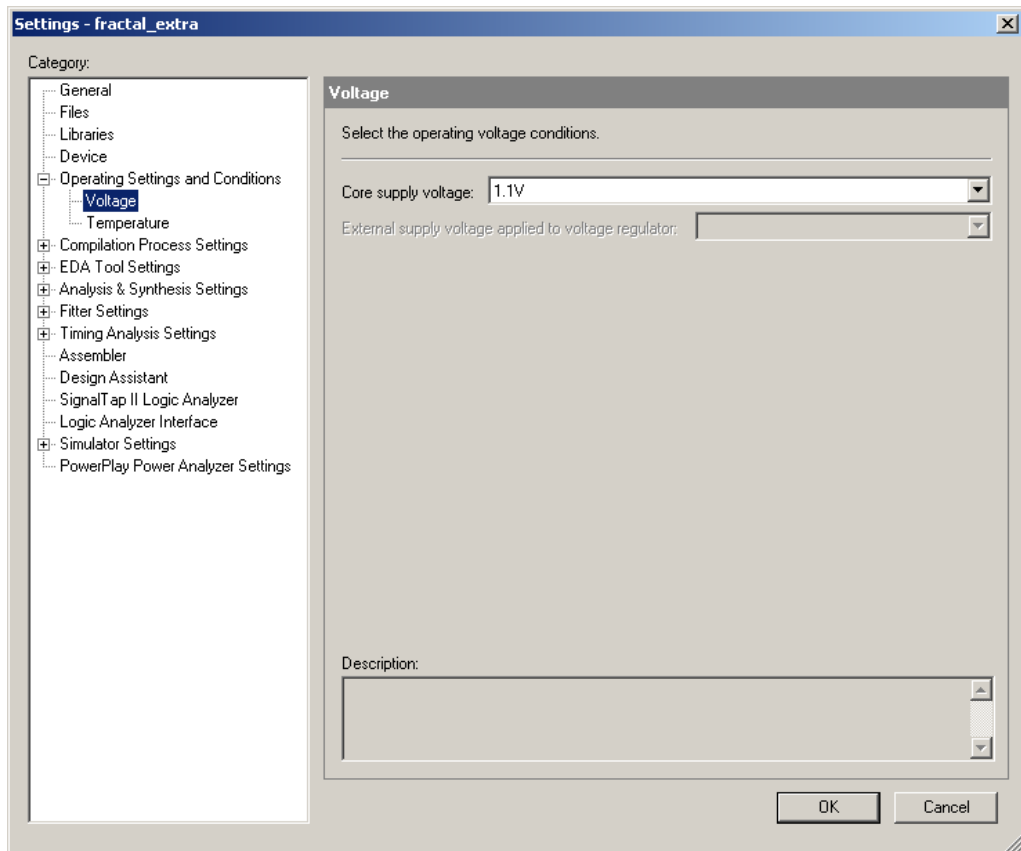


For more information about low power design techniques that can further reduce your design power usage by implementing changes at the design level, refer to the *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*.

## Selectable Core Voltage

The advanced architecture of Stratix III devices is capable of using 0.9 V or 1.1 V as the core supply voltage. Designers can select a suitable core supply voltage for their design based on performance and power requirements using the **Voltage** option available in the Quartus II software under the **Operating Settings and Conditions** category, as shown in [Figure 1](#).

**Figure 1. Operating Settings and Conditions Dialog Box**



The total power consumed by FPGA devices consists mostly of static power and dynamic power, as defined in the following formulas:

$$\text{Static Power} = \text{Voltage} \times \text{Current}$$



Static power has a significant dependency on voltage, as the static current is also a function of voltage.

$$\text{Dynamic Power} = \text{Capacitance} \times \text{Voltage}^2 \times \text{Frequency}$$

These equations show that voltage is the dominant factor in the power consumption of a device. Because voltage is a dominant factor, it is important to choose the right core supply voltage for your design. The core supply voltage provides power to Stratix III device logic resources, such as logic array blocks (LABs), Memory LABs (MLABs), DSP functions, memories, and interconnects. The 0.9 V core supply voltage produces lower static and dynamic power than the 1.1 V core voltage supply, which provides the highest performance. The PLLs and part of the I/Os (excluding the routing interface) must be powered with 1.1 V to provide the highest performance, and are not adjustable.



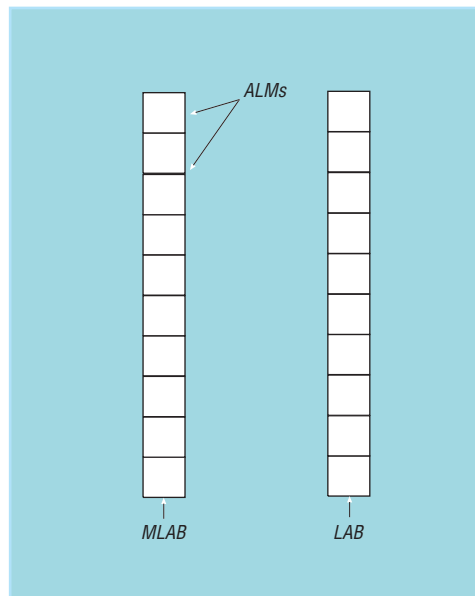
Refer to the *Programmable Power and Temperature Sensing Diode* chapter in the *Stratix III Device Handbook* for information about Stratix III core supply voltage and external power requirements.

## Programmable Power Technology


Programmable Power Technology enables Stratix III core logic to be programmed at the tile level for high-speed mode or low-power mode configuration. Tiles are defined as:

- A combination of a LAB and MLAB pair (including the adjacent routing associated with LAB and MLAB, as shown in [Figure 2](#))
- A DSP block
- A memory block

Tiles can be configured to operate in high-speed mode or low-power mode.

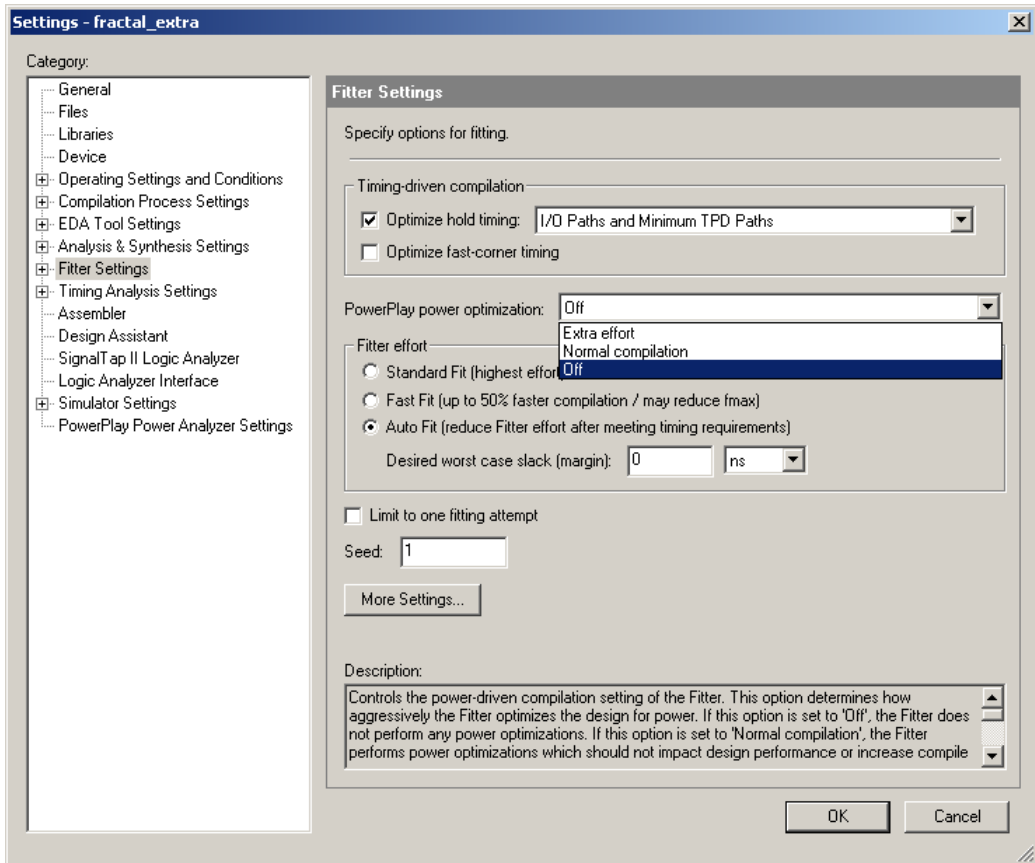
**Figure 2. Programmable Power Technology Tile View**

Tiles that are in the critical timing path of a design are configured in high-speed mode to meet the timing requirements. The remaining tiles are configured in low-power mode. A small percentage of the circuit uses the high-speed mode tiles. The remaining tiles are configured as low-power mode, resulting in a significant decrease in static power for low-power mode logic.

 External memory interface circuitry, PLLs, and the SERDES/DPA blocks cannot be configured in low-power mode. Memory and DSP blocks are configured in low-power mode only when they are unused.

The Quartus II software automatically controls which tiles operate in high-speed mode and which operate in low-power mode based on the timing constraint specified for the design. The **PowerPlay power optimization** option available in the **Fitter Settings** dialog box (Figure 3) controls the configuration of tiles in the high-speed mode or low-power mode, along with other power optimization techniques implemented at the Fitter level. You must provide realistic timing constraints for your design to achieve the lowest possible power consumption. After meeting your design performance goal, the Fitter employs extra effort to reduce the power consumption of your design, if you direct it to do so.

**Figure 3. Fitter Settings Dialog Box**



**Table 1** lists the settings for the **PowerPlay power optimization** option. These settings can only be applied on a project-wide basis. The **Extra effort** setting requires the Fitter to employ extensive effort to optimize the design for power, and can increase the compilation time.

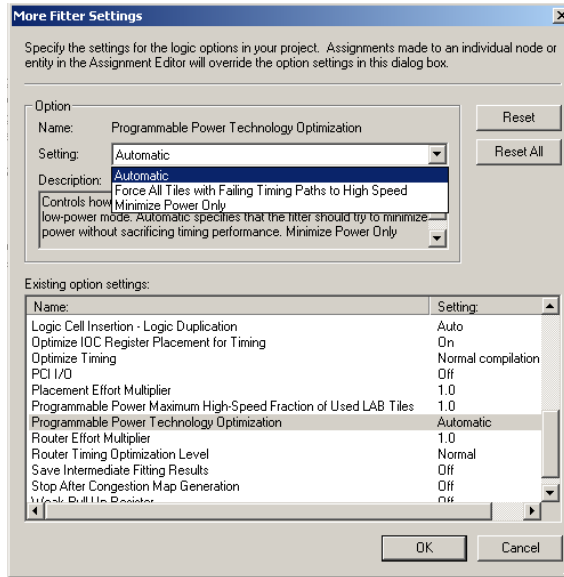
<b>Settings</b>	<b>Description</b>
Off	No netlist, placement, or routing optimizations are performed to minimize power.
Normal compilation (Default)	Enables power optimization techniques that are not expected to reduce design performance.
Extra effort	Enables additional power optimizations that can reduce design power.

The **Normal compilation** setting is selected by default, and configures each tile in high-speed mode or low-power mode based on the timing constraints entered for the design. The design's critical paths are identified and the tiles along those critical paths are configured as high-speed mode tiles to meet the timing constraints. The remaining tiles are configured in low-power mode to reduce the overall design power usage.

The **Extra effort** setting performs the functions of the **Normal compilation** setting and other place-and-route optimizations during fitting to fully optimize the design for power. The Fitter applies extra effort to minimize power, even after timing requirements have been met, by effectively moving the logic closer during placement to localize high-toggling nets, and using routes with low capacitance. It also looks for opportunities to configure more high-speed mode tiles into low-power mode tiles to reduce power consumption. However, this extra effort can increase the compilation time.

Another way to control the high-speed mode or low-power mode tile configuration is to enable the **Programmable Power Technology Optimization** and **Programmable Power Maximum High-Speed Fraction of Used LAB Tiles** options, available under the **More Settings** button in the **Fitter Settings** dialog box, as shown in [Figure 4](#).

**Figure 4. Programmable Power Technology Optimization Settings**



The available settings for the **Programmable Power Technology Optimization** option are **Automatic**, **Force All Tiles with Failing Timing Paths to High Speed**, and **Minimize Power Only**. **Automatic** is the default setting, and specifies that the Fitter use the power-driven Fitter option, as described in [Table 1](#). The **Force All Tiles with Failing Timing Paths to High Speed** setting sets all tiles with failing timing paths to high speed. The default setting, which is **Automatic**, can result in some of the paths in your design not meeting timing by setting tiles to low power, if these failing paths do not affect the speed of any clocks in your design. The **Force All Tiles with Failing Timing Paths to High Speed** setting sets all tiles with failing timing paths to high speed, and is useful during timing closure.

The **Minimize Power Only** setting specifies that the Fitter should set the maximum number of tiles to operate in low-power mode. This setting may impact design performance, but results in the largest power savings.

The default setting for the **Programmable Power Maximum High-Speed Fraction of Used LAB Tiles** option is 1.0. This option sets a limit on the number of high-speed tiles that can be used for your design. With the value set at 1.0, there is no restriction on the number of high-speed tiles, and the Fitter uses the minimum number needed to meet the timing

requirements of your design. Specifying a value lower than 1.0 may degrade timing quality, because some timing critical resources might be forced into low-power mode.

## Fitter Reports

The Fitter report section of the **Compilation Report** provides detailed information about the number of low-power mode tiles and LAB tiles used in the design. The **Fitter Resource Usage Summary** shows the Programmable Power Technology low-power tiles and Programmable Power Technology low-power LAB tiles usage information for Stratix III devices, as shown in [Figure 5](#). This information is further divided into actual low-power mode tiles and LAB tiles used by the design, as well as unused tiles and LAB tiles that are automatically configured in low-power mode by the Quartus II software.

**Figure 5. Fitter Resource Usage Summary**

Resource		Usage
59	Global clocks	1 / 16 ( 6 % )
60	Quadrant clocks	0 / 64 ( 0 % )
61	Periphery clocks	0 / 166 ( 0 % )
62	SERDES transmitters	0 / 88 ( 0 % )
63	SERDES receivers	0 / 88 ( 0 % )
64	Average interconnect usage	5%
65	Peak interconnect usage	30%
66		
67	Programmable power technology low-power tiles	2,407 / 2,957 ( 81 % )
68	-- low-power tiles that are used by the design	904 / 2,407 ( 38 % )
69	-- unused tiles (low-power)	1,503 / 2,407 ( 62 % )
70		
71	Programmable power technology low-power LAB tiles	1,580 / 2,130 ( 74 % )
72	-- low-power LAB tiles that are used by the design	871 / 1,580 ( 55 % )
73	-- unused LAB tiles (low-power)	709 / 1,580 ( 45 % )
74		

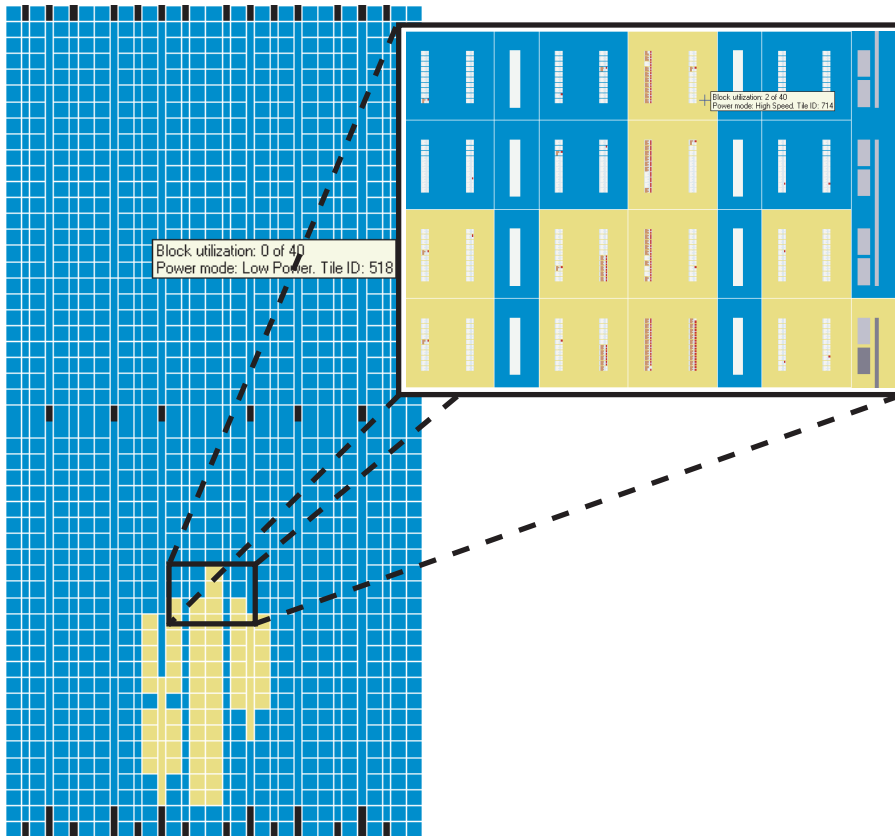
\* Register count does not include registers inside block RAM or DSP blocks.

## Chip Planner View

The Chip Planner tool in the Quartus II software enables you to view high-speed mode and low-power mode tiles implemented for your Stratix III design. To start the **Chip Planner**, on the **Tools** menu, click **Chip Planner**. The **Power Analysis (Assignment)** mode view setting under the **Layer set** option provides a hierarchical view of your design

implementation. This view shows the high-speed mode and low-power mode tiles used for your design in different colors to make it easier to distinguish between them, as shown in Figure 6.

**Figure 6. Chip Planner View with Power Analysis (Assignment) Mode**



When you place the cursor over a resource at this level, a tooltip appears that describes the power mode for that particular tile. The Chip Planner also enables you to view the internal structure of Altera devices and incrementally edit logic element (LE) and I/O cell configuration after place-and-route has been performed.



For more information about the Chip Planner tool, refer to the *Design Analysis and Engineering Change Management with Chip Planner* chapter in volume 3 of the *Quartus II Handbook*.

## Device Selection Considerations

Different device families have different power characteristics. Many parameters affect a device family's power consumption, including choice of process technology, supply voltage, electrical design, and device architecture. In addition to these parameters, power in the Stratix III family of devices is also affected by the speed grade selection. Speed grades describe the relative speed of each device. The lower the number, the faster the device. For example, the -2 speed grade device is the fastest, the -3 speed grade device is medium speed, and the -4 speed grade device is the slowest. For Stratix III devices, choosing a faster speed grade device can lead to increased performance and reduced static power for your design. This level of power saving is achieved by using the Programmable Power Technology, which reduces the number of high-speed mode tiles needed to meet timing in the faster speed grade device.

Faster speed grade devices may be beneficial in a variety of situations. For example, if you compile your design in a medium speed grade Stratix III device and meet your performance goal with 20% utilization of high-speed tiles, you can further reduce the power consumption of your design by selecting a faster speed grade device. The faster speed grade device allows you to meet your performance requirement and use fewer high-speed mode tiles than the medium speed grade device, reducing the total power consumption of your design.



If you meet your performance and power requirements by selecting a low operating voltage for your selected Stratix III device, there is no need to move to a faster speed grade device. However, if the absolute lowest power is required, move to a faster speed grade device, which will result in higher performance and the lowest possible power consumption.

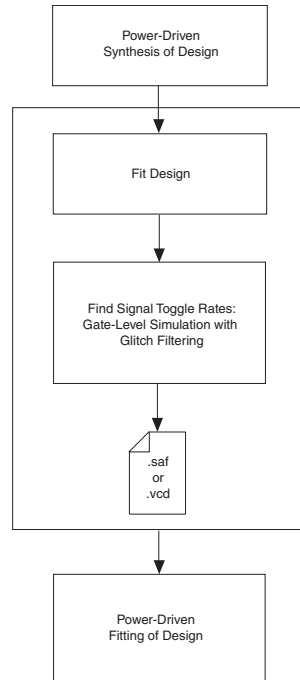


For more information about device selection considerations, refer to the *PowerPlay Power Analysis* chapter in volume 2 of the *Quartus II Handbook*.

## Quartus II PowerPlay Power Optimization Flow

The recommended design flow to fully optimize a design for power during compilation using the Quartus II software is shown in [Figure 7](#). This flow uses the power-driven compilation options available in the Quartus II software.

**Figure 7. Recommended Design Flow for Power-Driven Compilation**



The power-driven compilation takes place at the synthesis and Fitter levels. Power-driven synthesis changes the synthesis netlist to optimize the design for power. Power-driven synthesis settings perform memory optimization and power-aware logic mapping during synthesis. The power-driven Fitter (**Extra effort** setting) performs place-and-route optimization and controls the high-speed mode or low-power mode tiles configuration during fitting to fully optimize the design for power, as described in the “[Programmable Power Technology](#)” section.



For more information about power-driven compilation and low-power design techniques, refer to the [Power Optimization](#) chapter in volume 2 of the *Quartus II Handbook*.

Accurate toggle-rate data information on each signal in your design is important for optimizing design power during place-and-route. The power-driven Fitter uses this information to guide the Fitter and optimize the design power based on the signal activity information of the design. The most accurate signal activity provides the best power optimization during fitting. Signal activities from full, post-fit netlist (timing) simulation provide the highest accuracy, because all node activities reflect actual design behavior, if supplied input vectors are representative of typical design operation. To use the signal activities information from post-fit simulation you must compile the design using the default settings (**Normal compilation**). Simulate your design using gate-level simulation and generate a signal activity file (**.saf** or **.vcd**) for the design. Recompile the design using the power-driven fitting (**Extra effort**) that uses the design signal activities information to further optimize the design for power, as shown in [Figure 7](#). This procedure makes the design flow a bit more time consuming but is very effective for design power optimization.



For more information about how to create a signal activities file (**.saf** or **.vcd**), refer to the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

## Conclusion

Historically, performance has been the main criterion in selecting an FPGA. With the introduction of 65-nm technology, power consumption is fast becoming a critical selection criterion. To accommodate this newly introduced design constraint, Stratix III devices are designed to allow low power consumption without compromising performance. Innovative Programmable Power Technology and Selectable Core Voltage options provide the best combination to offer designers the choice of performance circuitry versus low-power mode circuitry.

## Referenced Documents

This application note references the following documents:

- *Design Analysis and Engineering Change Management with Chip Planner* chapter in volume 3 of the *Quartus II Handbook*
- *Power Optimization* chapter in volume 2 of the *Quartus II Handbook*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Programmable Power and Temperature Sensing Diode* chapter in the *Stratix III Device Handbook*

# Document Revision History

Table 2 shows the revision history for this document.

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
August 2007 v2.0	<ul style="list-style-type: none"> <li>• Replaced <a href="#">Figures 1, 2, 3, and 4</a>.</li> <li>• Removed “column I/O interface” reference.</li> <li>• Made several changes to <a href="#">Table 1</a>.</li> <li>• Added new text in “<a href="#">Programmable Power Technology</a>” section.</li> <li>• Made several minor text edits.</li> <li>• Created hypertext links to referenced external documents.</li> </ul>	—
November 2006 v1.0	Initial Release	—



101 Innovation Drive  
San Jose, CA 95134  
www.altera.com  
Literature Services:  
literature@altera.com

Copyright © 2007 Altera Corporation. All rights reserved. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.



I.S. EN ISO 9001