

Altera Delivers Customer-Driven Innovation

Keeping a keen eye on the needs of the customer, Altera takes innovative steps in the successful development of next-generation FPGAs

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Along with higher densities and better performance, semiconductor users have become accustomed to reduced power consumption as core voltage is reduced with every process technology node. Developing new ways to manage power with each new generation of programmable logic technology has always been a key component of Altera's research and development efforts, especially as the pattern of power reduction began changing at the 90-nm node due to leakage issues. With the density of FPGAs doubling from 130-nm and gate oxides becoming thinner, Altera made a number of innovations in its 90-nm FPGAs and development tools to help customers overcome power consumption issues. At the 65-nm node, where power is an even more critical issue than at 90-nm, Altera has identified an opportunity to create an architecture offering substantial power savings while still delivering the density and performance benefits of the new process. This is of critical importance to our customers as they place a greater priority on productivity, time to market, and cost of ownership than ever before in their pursuit to be profitable in an increasingly competitive market environment.

The Days of Deep Pockets Are Over

In the days of the Internet bubble, it seemed as if though money was no object. The only thing a company really cared about was its ability to introduce products to market as quickly as possible. There were few price pressures, so product cost was not an issue, and companies could easily raise money and hire employees, so neither was development cost. Big and small companies alike, especially in the communications market, were totally focused on new product development and introduction. This was an exceptional period for the FPGA industry, since FPGAs provide maximum flexibility, the ability to innovate and differentiate, and enable very quick time to market.

After the bubble burst, raising funds suddenly became difficult and companies had to be profitable, or at least show a clear path toward turning a profit. With the money taps

turned off, FPGA customers—those who survived—became concerned with product costs. In response, Altera led the FPGA industry with the introduction of the Cyclone® FPGA family, optimized from the ground up for low cost, and opening up vast opportunities for high-volume applications to reap the benefits of programmable logic. By staying focused on the electronic industry's need for low-cost programmable logic that can replace ASSPs with their flexibility constraints and ASICs with their high development costs, Altera expects this trend to continue as it gears up to introduce its next generation Cyclone family.

Today's Customer Requirements: Higher Productivity and Lower Risk

While flexibility, time to market, and cost continue to be very important, today's customers are increasingly concerned about improving productivity and lowering risk. To be competitive, companies need to develop more products that are more complex as they face shorter time to market and time in market. However, they have limitations on growing their research and development budgets. Therefore a key challenge facing every company today is how to do more with less. At the same time, the cost of any error is huge. Slipping a schedule, missing a market window, failing to deliver exactly what the market needs or introducing a product that is inferior to what competitors offer can be devastating.

3D: Define, Design, Deliver

Everything Altera does is with the customer in mind. Our customers want high levels of productivity with low levels of risk. They want the ability to innovate, to get their products to market quickly and they want superior product quality. This is why Altera puts significant effort into customer-centric product definition, design and delivery.

The key challenge in defining a new product is to find a balance between meeting the needs of the majority of customers and leaving out features that few customers will use. Designing unnecessary features into our programmable logic devices only leads to higher product cost and risk for our customers.

Altera uses very thorough design methodologies to ensure we provide high quality products on schedule. We work closely with our foundry partner TSMC to ensure we use

their processes properly and we make extensive use of test chips to verify new product designs before launching the product itself.

To ensure consistent product delivery, Altera has used a patented redundancy technology for many years that allows us to deliver high-density products at high volumes even early in the product life cycle. We also work closely with TSMC on an aggressive defect-density reduction program to continuously improve yields.

A good example of Altera's approach can be found with the Stratix® II GX FPGA family with embedded transceivers. Introduced in the fourth quarter of 2005, these devices are already shipping and used by a variety of customers. We chose to implement 6.375-Gbps transceivers, and as a result, Stratix II GX FPGAs feature the lowest power consumption and best signal integrity in the industry. The test chips Altera designed and validated before the Stratix II GX introduction allowed us to launch a product that worked right the first time.

The Next Challenge: 65 nm

Naturally, the move to 65 nm brings the Moore's law benefits of increased density and performance. However, at this process node, power consumption becomes a critical factor. Altera continues to address this challenge with a combination of process technologies, architectural innovations and development tools that enable customers to get the performance they need while keeping power consumption to a minimum. For example, customers should expect the 65-nm Stratix III family to deliver significantly higher density with as much as a 20 percent performance boost, and power savings that range from 30 to 70 percent compared to the 90-nm Stratix II.

Just the Right Performance—Automatically

In analyzing many customer designs during the definition process for our next-generation FPGAs, Altera found that only 5 to 40 percent of a typical design netlist requires high performance. The majority of the design could be implemented with low power and slow circuits, and still meet timing requirements. The exact amount of high-performance logic versus low-performance logic varies from design to design.

With this in mind, the 65-nm architecture was designed to offer customers the performance they need with the lowest possible power consumption. Parts of the FPGA can run at high performance and other parts can run at lower performance, and thus consume much less power. Moreover, any logic that is not needed by the design can be programmed to power down, further reducing power. What is exceptional about Altera's implementation is that the Quartus® II design software does all of this automatically. During compilation, the software configures some blocks to run at high performance and some to run at low power. In this way the customers automatically get the performance they require with the lowest possible power.

Design Software Is Critical

One of the key aspects of Altera's design methodology is that we design hardware and software simultaneously, so each can take full advantage of the other. The PowerPlay capabilities of the Quartus II development software optimize power in three phases.

First, the Quartus II software performs a power-aware synthesis. "Power aware" means that the software can minimize the number of RAM blocks accessed at each clock cycle, or can rearrange the design to eliminate high-toggling logic.

After the power-aware synthesis is complete, the Quartus II software performs power-aware placement and routing. It routes signals to minimize capacitance, or creates power-efficient DSP block configurations. Lastly, the assembler places unused areas of the FPGA in a power-down state.

Since its first 65-nm test chip taped out in April 2003, Altera has produced a series of test chips to carefully evaluate different circuits, modules and design techniques. As a result, Altera is on track to introducing its first 65-nm products later this year, with volume production in 2007. Altera will announce further product details later this year.

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